Optimal PHY Transceiver Techniques for 16 GT/s and Beyond

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Synopsys

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Agenda

- **Going Beyond 16 GT/s**
- **Challenges of PCI Express® Designs at 32 GT/s**
- **PHY Architectural Enhancements**
- **System Simulation Results**
- **Key PHY Features for Optimal System Solution**
- **Summary**

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PCIe® Announcement

- PCI–SIG announced 32 GT/s as its next evolution to surpass industry needs
- High-performance applications
  - Artificial Intelligence
  - Machine Learning
  - Gaming
  - Visual Computing
  - Storage
  - Networking
  - …
- Higher bandwidth is targeted to serve accelerator and GPU attachments, as well as constricted form factor applications.

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PCI-SIG® Fast Tracks Evolution to 32GT/s with PCI Express 5.0 Architecture

PCIe 5.0 Revision 0.3 specification now available to members

PCI-SIG Developers Conference 2017, Santa Clara, CA. – June 7, 2017 - PCI-SIG®, the organization responsible for the widely adopted PCI Express® (PCIe®) industry-standard input/output (I/O) technology, today announced 32GT/s as the next progression in speed for the PCIe 5.0 architecture, targeting high-performance applications such as artificial intelligence, machine learning, gaming, visual computing, storage and networking. Slated for completion in 2019, the specification development is well underway with Revision 0.3 already available to PCI-SIG member companies.

"In our 25-year history, PCI-SIG has maintained its commitment to our rigorous specification development process, while delivering specifications that are in lock-step with industry requirements for high-performance I/O," said Al Yanes, PCI-SIG Chairman and President. "PCIe 5.0 technology is the next evolution that will set the standard for speed, and we are confident that its 32GT/s bandwidth will surpass industry needs."

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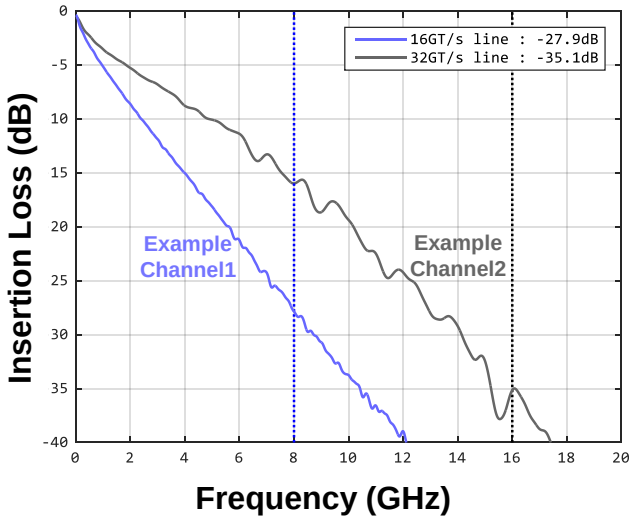
16 GT/s vs. 32 GT/s

- **PCIe 5.0 doubles data-rate: 16 GT/s to 32 GT/s**
  - Nyquist frequency also doubles from 8 GHz to 16 GHz
- **Challenges**
  - Channel insertion loss:
    - ~35 dB @ 16 GHz Nyquist vs ~28 dB @ 8 GHz Nyquist
  - Cross talk increases with frequency due to capacitive coupling
  - Ratio of signal to interference is higher @ 32 GT/s

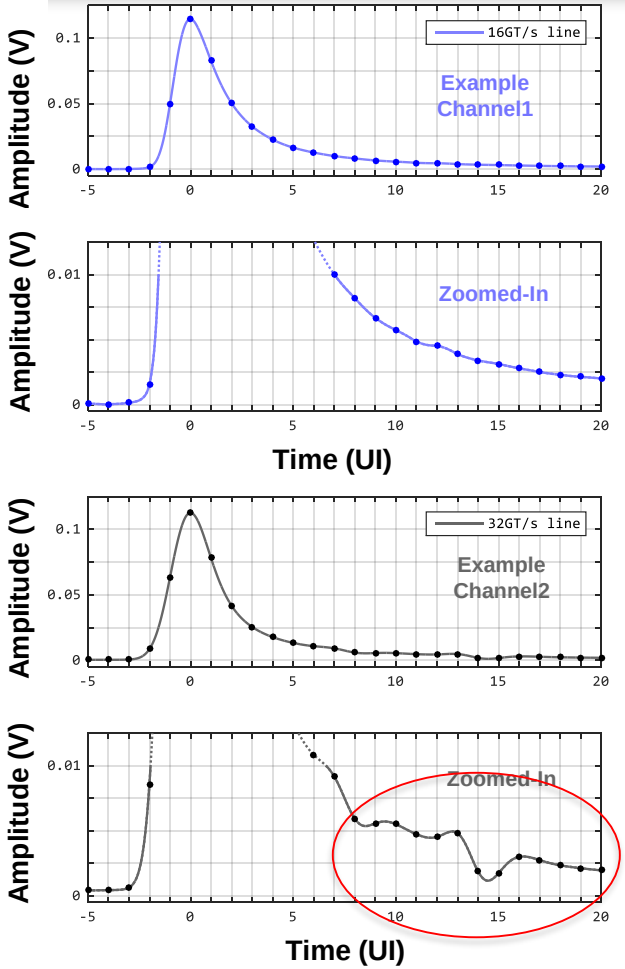


Frequency Domain Representation: Plot illustrating insertion loss for two different example channels at Nyquist frequency

16 GT/s vs. 32 GT/s

Single-Bit Response

- Doubles the electrical length of any discontinuities in the channel
- Physically the distance to the discontinuities may remain constant, however electrically it is twice the number of UIs
- Discontinuities / residual ISI (at higher number of UIs e.g. 10+) is usually not addressed by Analog Front End (AFE) and requires DFE taps



Time Domain Representation: Plot illustrating single UI through the channel, with no TX Equalization and ideal TX

16 GT/s vs. 32 GT/s

Example RX AFE budgeting

- With launch amplitude, TX EQ, channel loss, desired RX sampler input amplitude we can start to derive targets for:
  - DC/HF Gain, Boost, DFE Tap-1
- **16 GT/s link**
  - Input signal at Nyquist rate is 20 mVpk
  - Assuming RX post-eq target of 125 mVpk and max DFE tap-1 of 50 mV
  - RX front-end must provide 11.4dB of gain @ Nyquist and 10.7dB of Boost (HF minus LF gain)
- **32 GT/s link**
  - Input signal to RX at Nyquist rate is just 9 mVpk
  - Using the same post-eq target of 125 mVpk would require 18.4 dB of gain @ Nyquist
    - Need multiple stages and each stage would limit overall bandwidth
  - Mitigated partially by using a larger DFE tap-1
    - By increasing DFE tap-1 to 80mV, Nyquist gain requirement is reduced to 13.9 dB and total Boost required is 11.8 dB
- **What about Bandwidth?**
  - AFE bandwidth @ 32 GT/s RX nearly doubles

32 GT/s AFE requires higher gain and boost, twice Bandwidth

16GT/s RX budget

INPUTS		
pre (dB)	3.5	Preset P7
post(dB)	6	
txamp (mVpk)	400	
max dfe1(mV)	50	
ref target(mV)	125	
channel loss at DC	0	
channel loss at Nyquist	-28	

RESULT	signal at rx input (mVpk)	afe out target (mVpk)	required AFE gain (dB)
DC	160.5	175.0	0.7
Nyquist	20.3	75.0	11.4

32GT/s RX budget

INPUTS		
pre (dB)	3.5	Preset P7
post(dB)	6	
txamp (mVpk)	400	
max dfe1(mV)	80	
ref target(mV)	125	
channel loss at DC	0	
channel loss at Nyquist	-35	

RESULT	signal at rx input (mVpk)	afe out target (mVpk)	required AFE gain (dB)
DC	160.5	205.0	2.1
Nyquist	9.1	45.0	13.9

16 GT/s vs. 32 GT/s

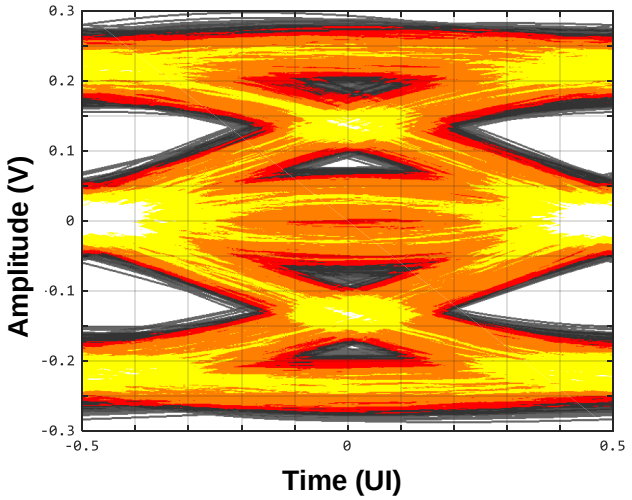
Limitations of 16 GT/s behavioral EQ

- 16 GT/s behavioral RX equalizer:1st Order CTLE

$$H(s) = \omega_{P2} \frac{s + \omega_{P1} * A_{DC}}{(s + \omega_{P1}) * (s + \omega_{P2})}$$

$\omega_{P1} = 2\pi * 2\ \text{GHz}$ $\omega_{P2} = 2\pi * 16\ \text{GHz}$

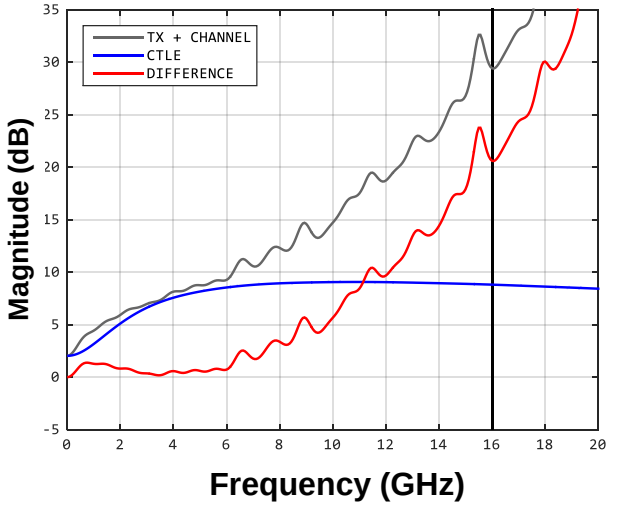
A_{DC} ranges from -6 to -12 dB in 1.0 dB steps



- Building 32 GT/s behavioral EQ by scaling the pole frequencies

$\omega_{P1} = 2\pi * 4\ \text{GHz}$ $\omega_{P2} = 2\pi * 32\ \text{GHz}$

  - Ideally, CTLE should match the inverse of the channel response
  - Scaling the EQ alone not enough, there is significant difference between CTLE and inverse channel response above 6GHz



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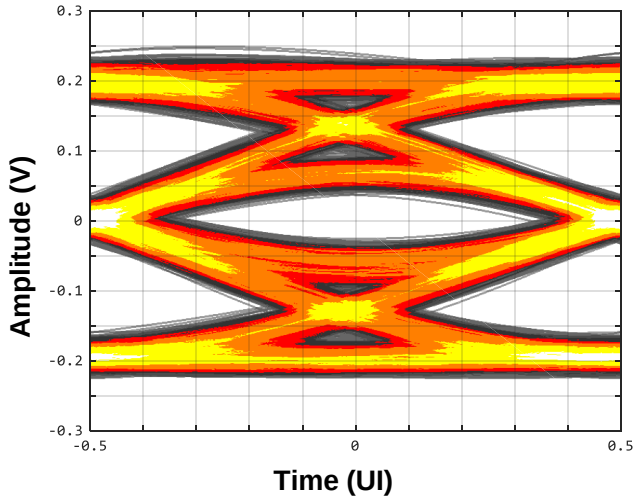
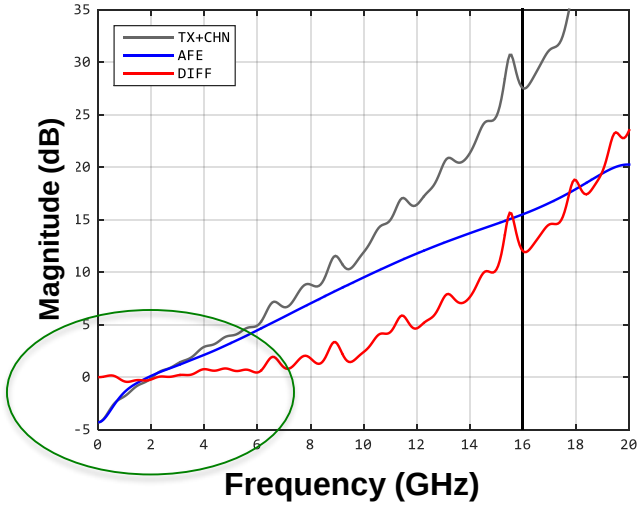
PHY Architectural Enhancements

AFE Low Frequency Equalization

- Channel losses include
  - Resistive losses ($\propto\sqrt{f}$) at lower frequencies
  - Dielectric losses ($\propto f^2$) at higher frequencies
- 32 GT/s dielectric losses become significant and must be equalized
- 16 GT/s behavioral RX CTLE cannot fit both resistive and dielectric loss regions
- Adding a low frequency pole-zero pair to AFE transfer function provides additional degrees of freedom
  - Un-equalized dielectric can be equalized w/ DFE





PHY Architectural Enhancements

Bandwidth Extension Techniques

- Doubling of the AFE bandwidth requires circuit implementation changes
- The following are potential solutions, each with their relative merits & costs

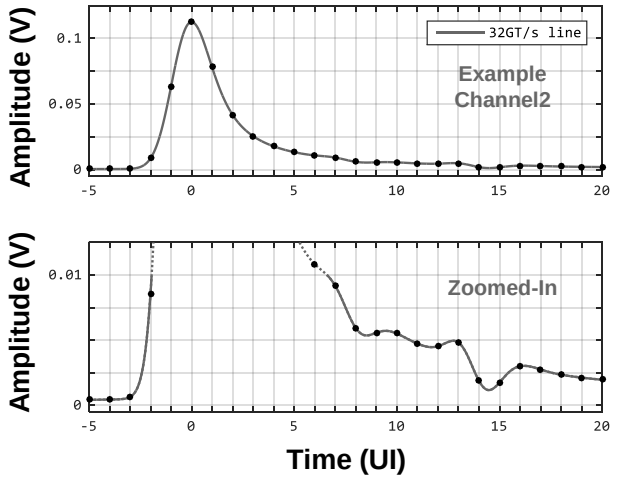
Technique	Negative Miller Capacitor	Cherry-Hooper	Inductive Peaking (Active)	Inductive Peaking (Passive)
Area	+	+	+ +	− −
Power	+	− −	+	+ +
Noise	−	− −	−	+
Linearity	−	−	−	+ +

PHY Architectural Enhancements

What About DFE?

- Practical 16 GT/s PHY RX typically uses 3-5 taps
  - Behavioral RX Equalizer only uses 2-tap DFE

- With increased channel loss, ISI, and discontinuities at larger electrical distances come the need for several practical changes to the DFE:
  - Increased tap-1 value
  - Increased number of fixed taps
  - The possibility of floating taps

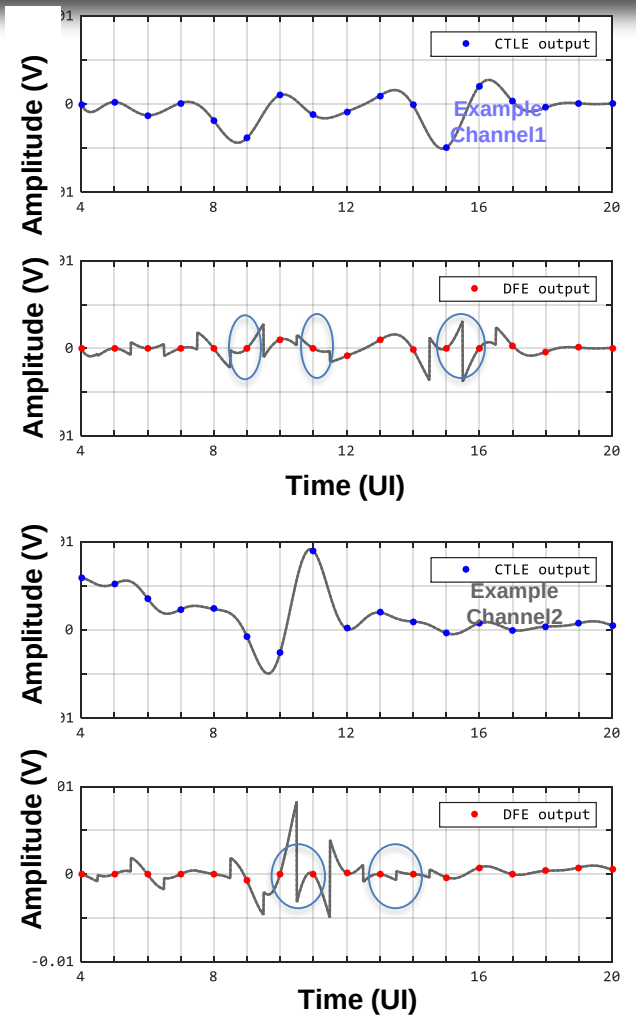


Time Domain Representation:
Plot illustrating single UI through the channel, with no TX Equalization and ideal TX

PHY Architectural Enhancements

Floating Taps

- Floating taps to catch impact of reflections in the channel from farther out
- Taps must “float” since distance to these points will vary from channel to channel
- Design cost to floating taps



Example: 8 fixed taps, 4 floating taps

PHY Architectural Enhancements

Why Can't We Make DFE tap-1 Higher?

- Increasing maximum value of DFE tap-1 eases the gain requirements of CTLE

- Practical limitations on maximum DFE tap-1 value
  - DFE taps are only set after RX adaptation has occurred; but this can only happen after the CDR has locked to the incoming signal
    - Sufficient equalization must provided by AFE without DFE tap-1
  - DFE operates by taking previous bit decisions and multiplying them by tap weights in order to adjust the adjust/correct the current bit decision
    - Small input signal may lead to decision errors
    - With Large tap-1 weight, error can propagate through DFE taps
    - Number of DFE taps increased @ 32 GT/s
    - Result can be a burst of consecutive bits in error

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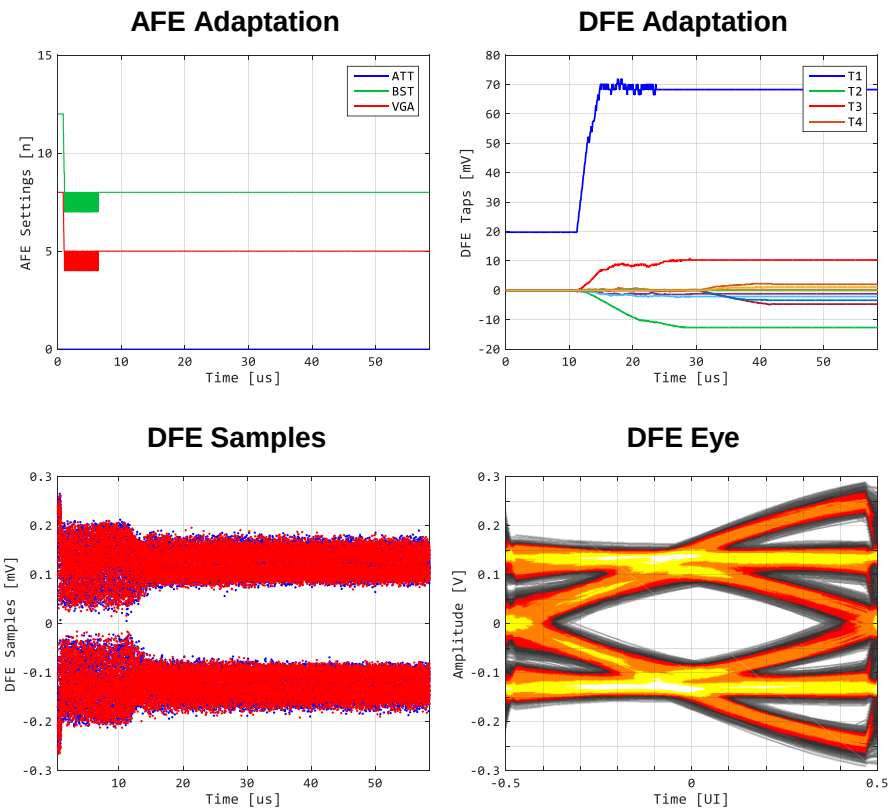
System Simulation Results

- Time-step model of system (TX to RX)
- AFE adaptation optimizes Boost (BST) and gain (VGA) settings according to channel
- DFE adaptation selects floating tap positions and optimizes fixed and floating tap values
  - DFE tap-1 is 70mV
  - Additional fixed taps improve eye height by 30 mV
  - Floating taps improve eye margin by an additional 15 mV



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Key Features for System Designers

- Multiple techniques must be employed for robust 32 GT/s PHY solutions
  - Wide bandwidth circuit architectures
  - CTLE with the ability to match inverse channel response across wide range of frequencies
  - Increased number of fixed DFE taps
  - Floating DFE taps to compensate for electrical discontinuities farther out from the main bit pulse
  - Adaptation algorithms to track changes temperature & voltage
- Shorter links may allow for further PHY power optimizations
  - Configurable DFE option
- PCIe 5.0 standard is developing/deploying quickly, a flexible PHY solution is needed for early systems

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Summary

- Going beyond 16 GT/s
  - Why: Explosion of Artificial Intelligence, Datacenters, Cloud, IoT driving need for higher throughput
- Challenges of PCI Express Designs at 32 GT/s
  - Physical constraints
  - Electrical constraints
    - Insertion loss
    - Crosstalk
  - Limitations of 16 GT/s Ref EQ
- PHY Architectural Enhancements
  - AFE improvements
  - Bandwidth extension techniques
  - Configurable DFE
- System Simulation Results
- Key PHY features for Optimal System Solution
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Contributors

- **Phil Chopp**
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